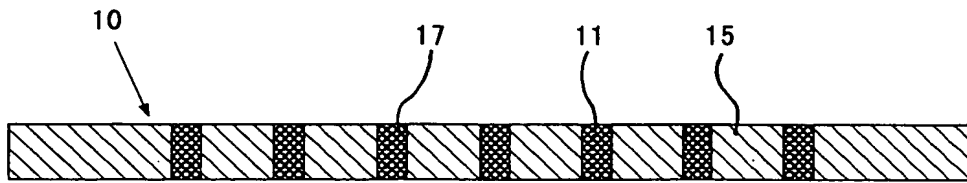
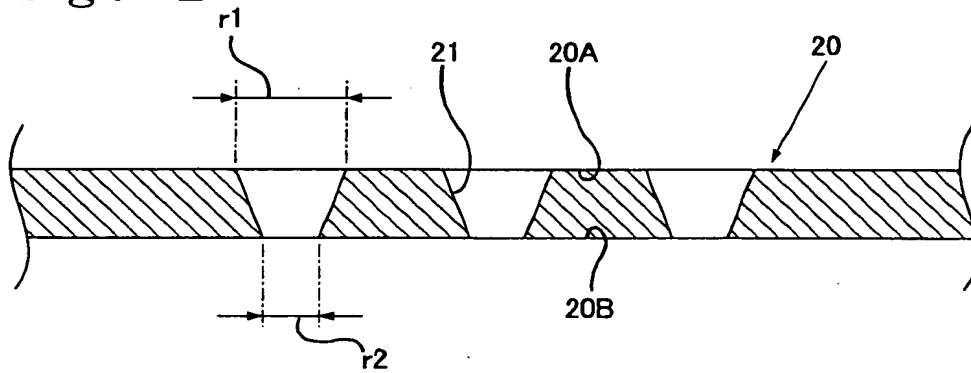


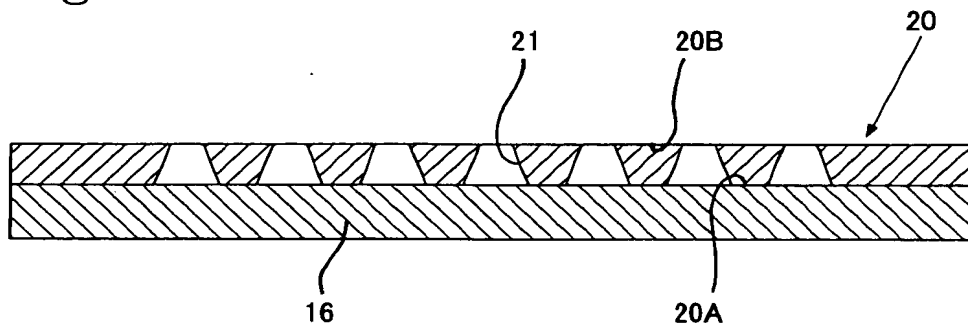
F i g . 1



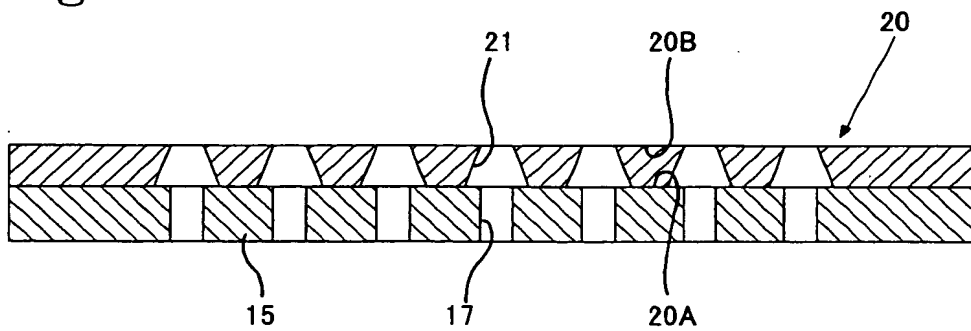
F i g . 2



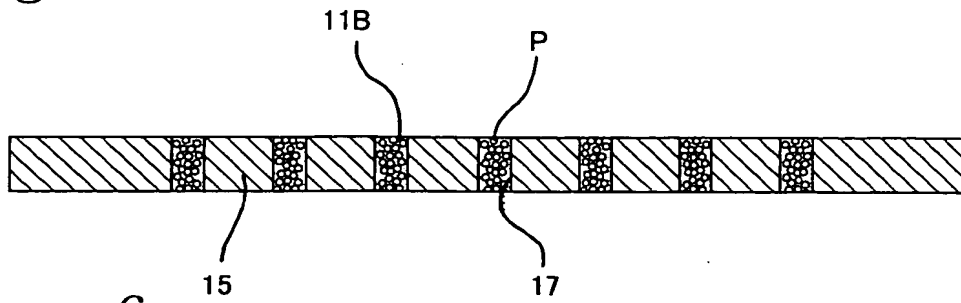
F i g . 3



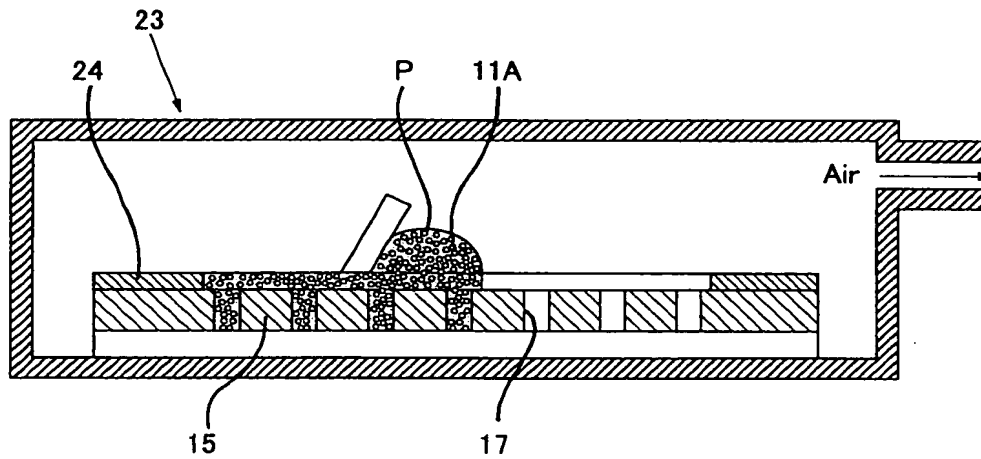
F i g . 4



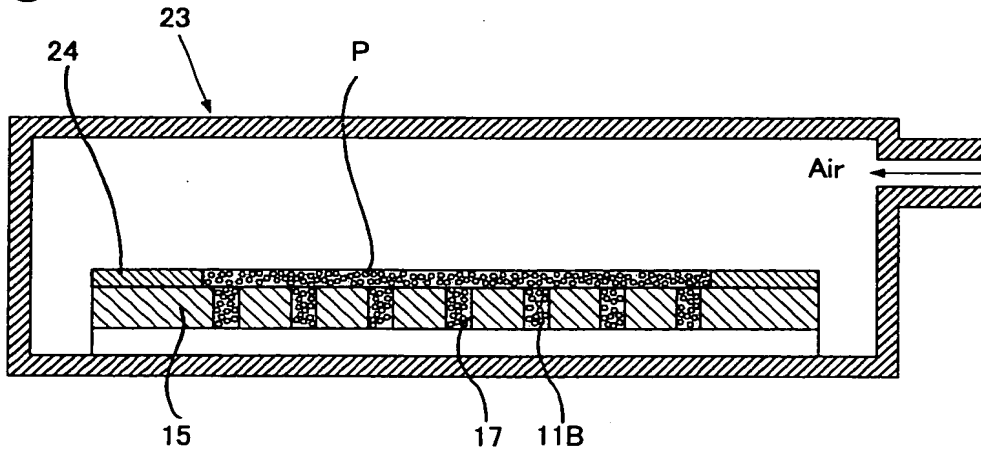
F i g . 5



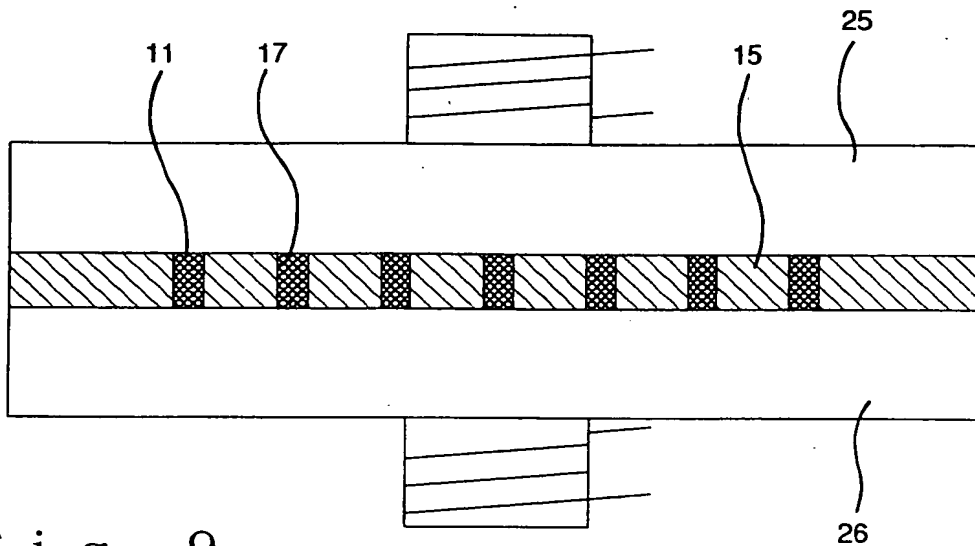
F i g . 6



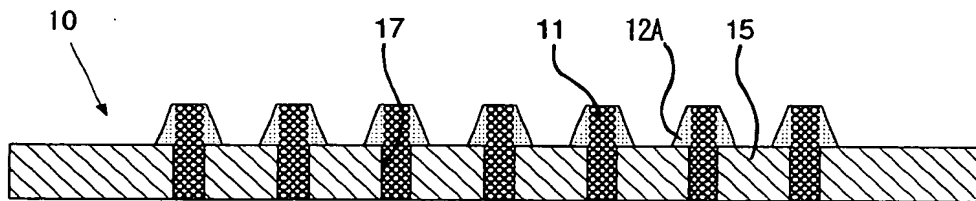
F i g . 7



F i g . 8



F i g . 9



F i g . 10

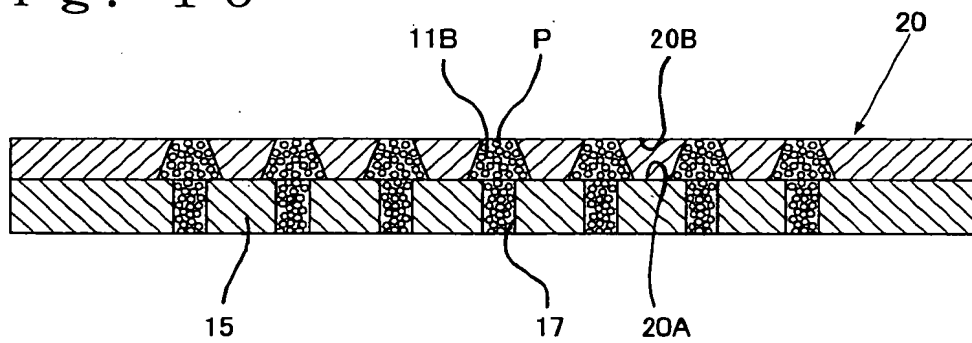


Fig. 11

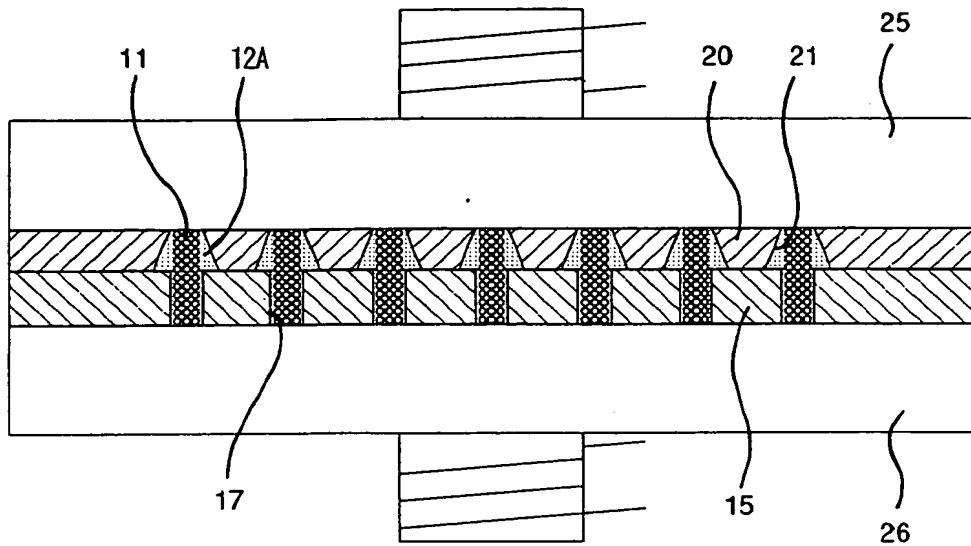


Fig. 12

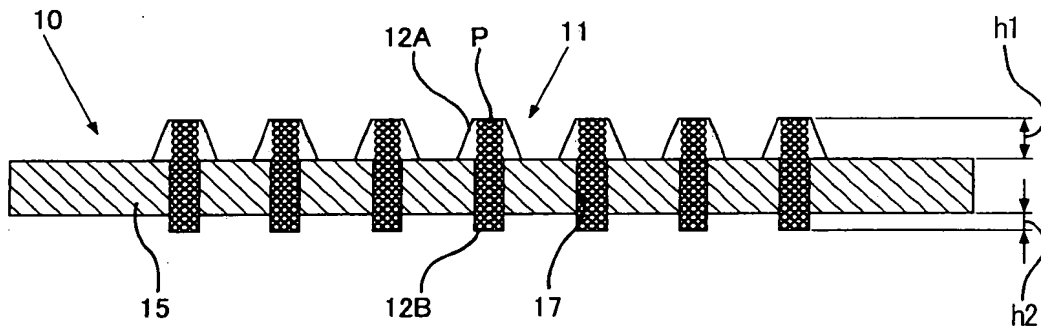


Fig. 13

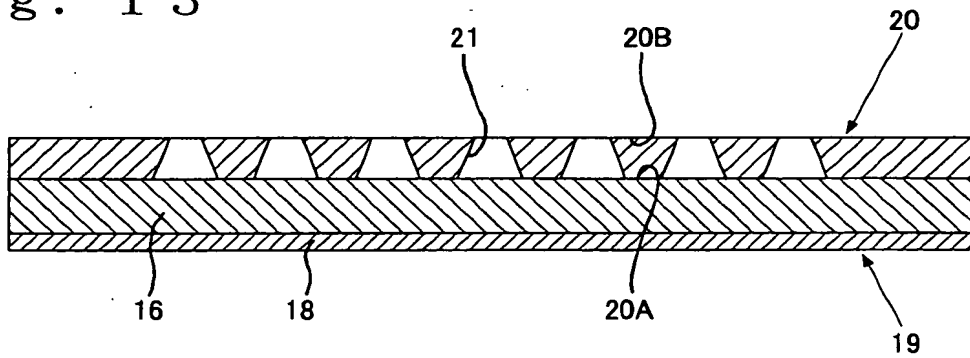
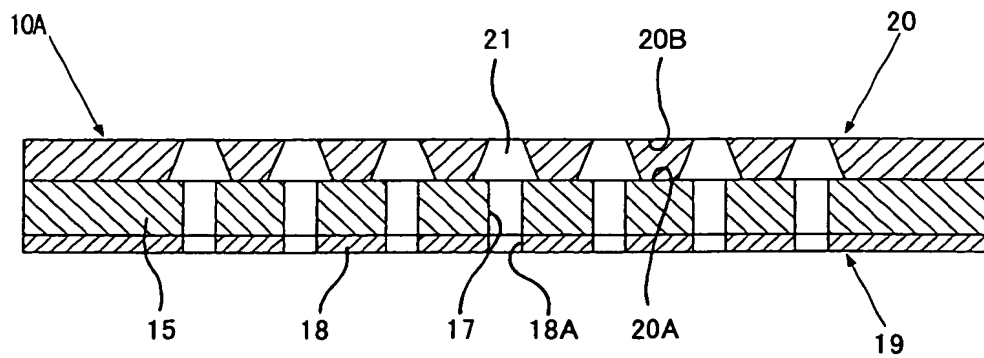
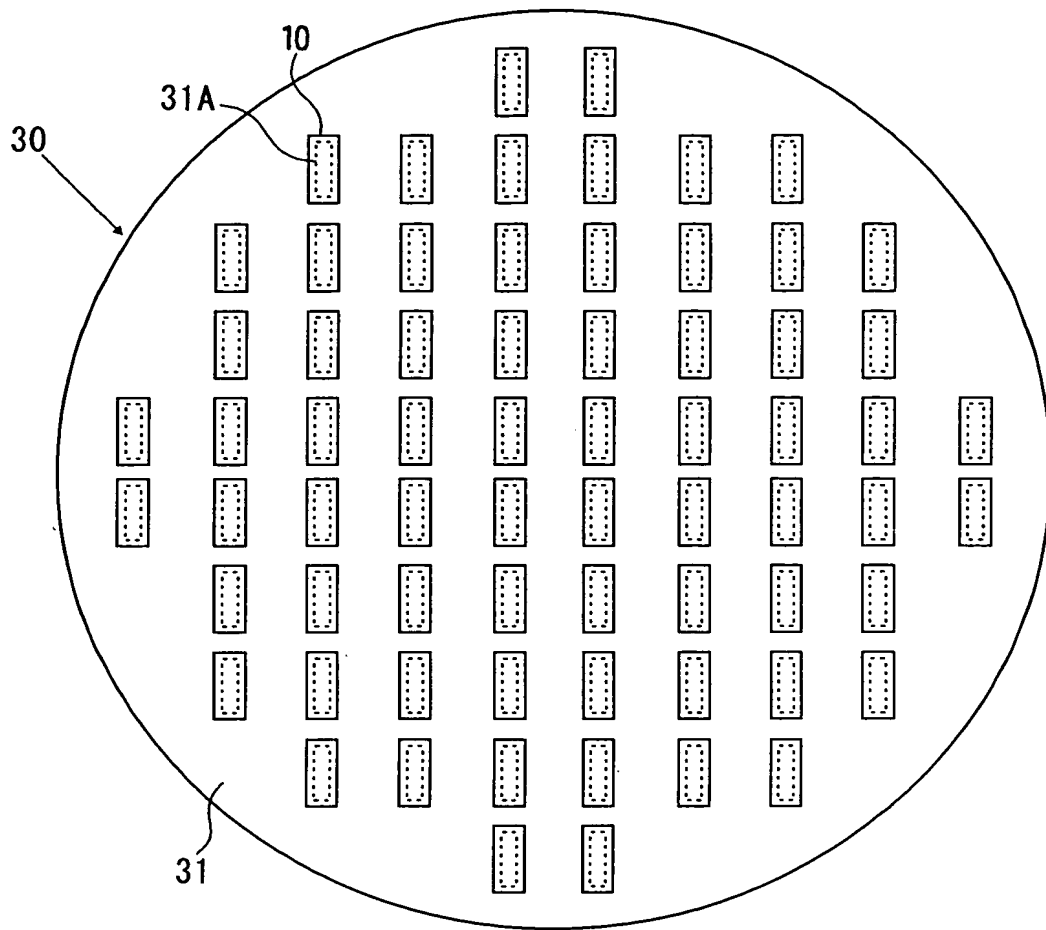


Fig. 14

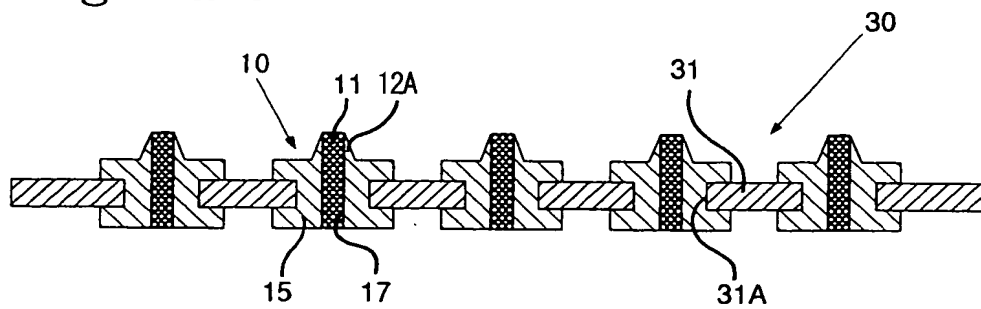


A cross-sectional view of a semiconductor device 11. The device consists of a substrate 15 with a series of vertical pillars 12A. The pillars are connected by a horizontal layer 18. The entire structure is mounted on a base 18. The device is shown in a cross-section with a dashed line indicating a boundary or interface.

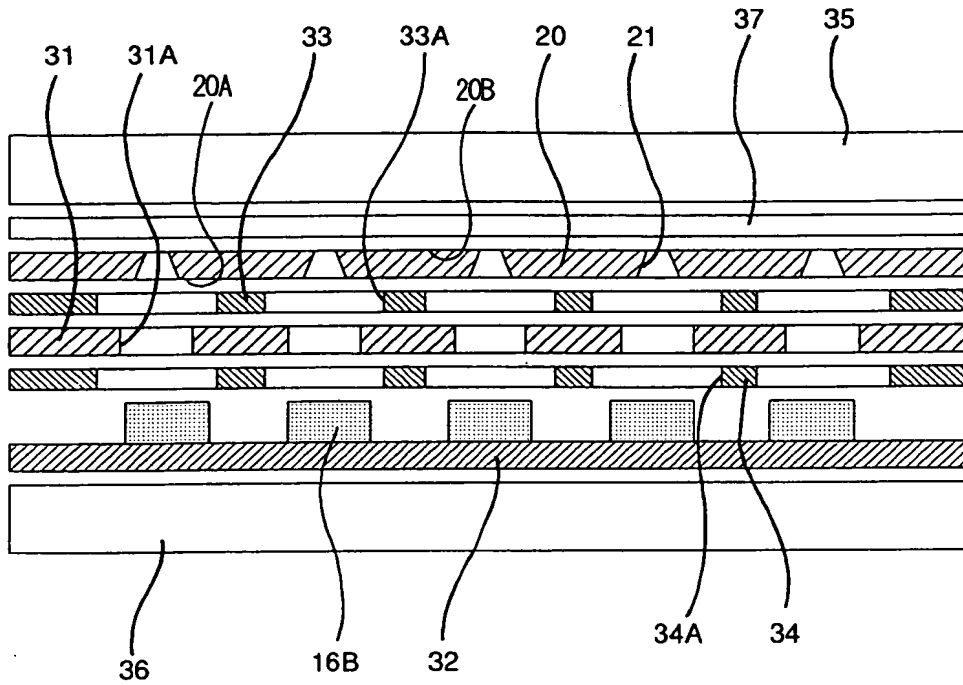
F i g . 1 8



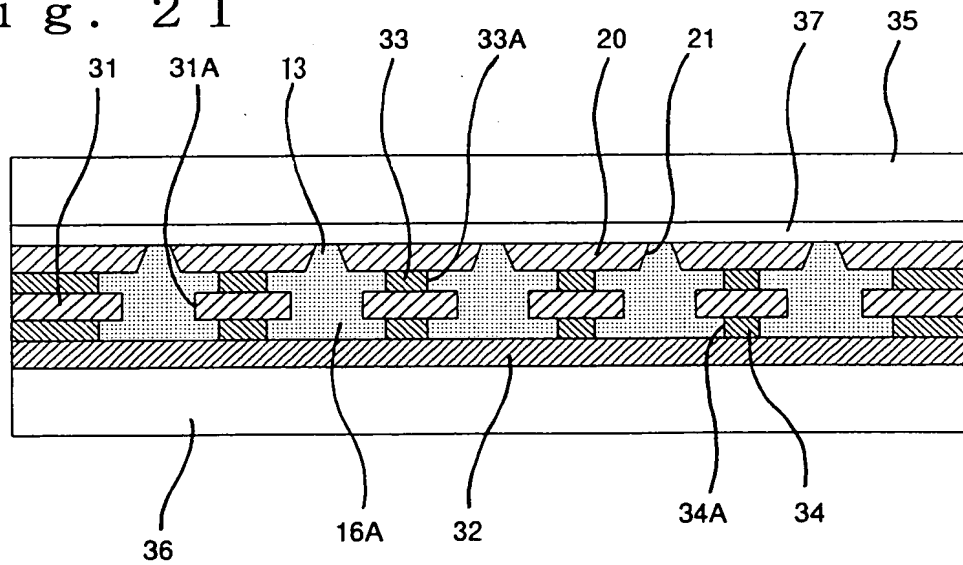
F i g . 1 9



F i g . 2 0



F i g . 2 1



F i g . 2 2

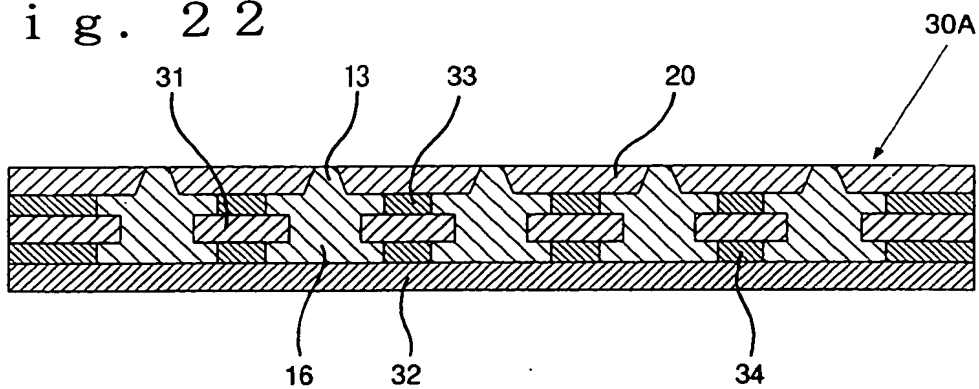


Fig. 23

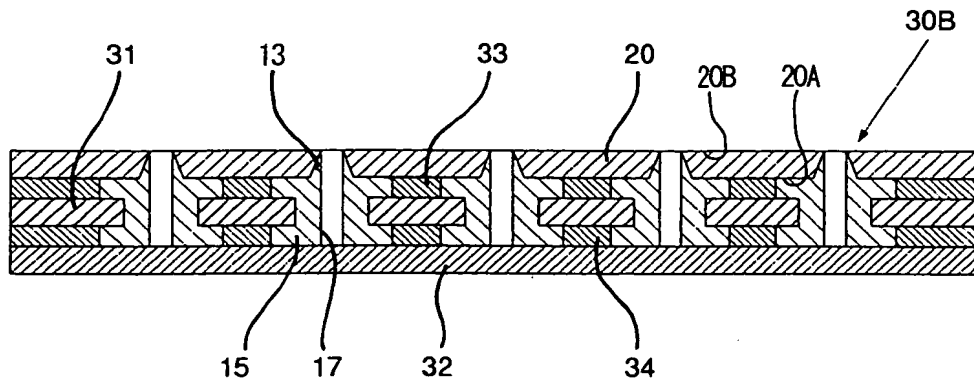


Fig. 24

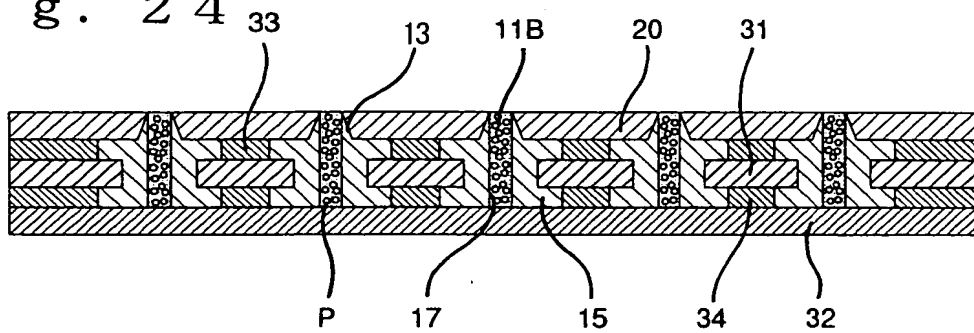
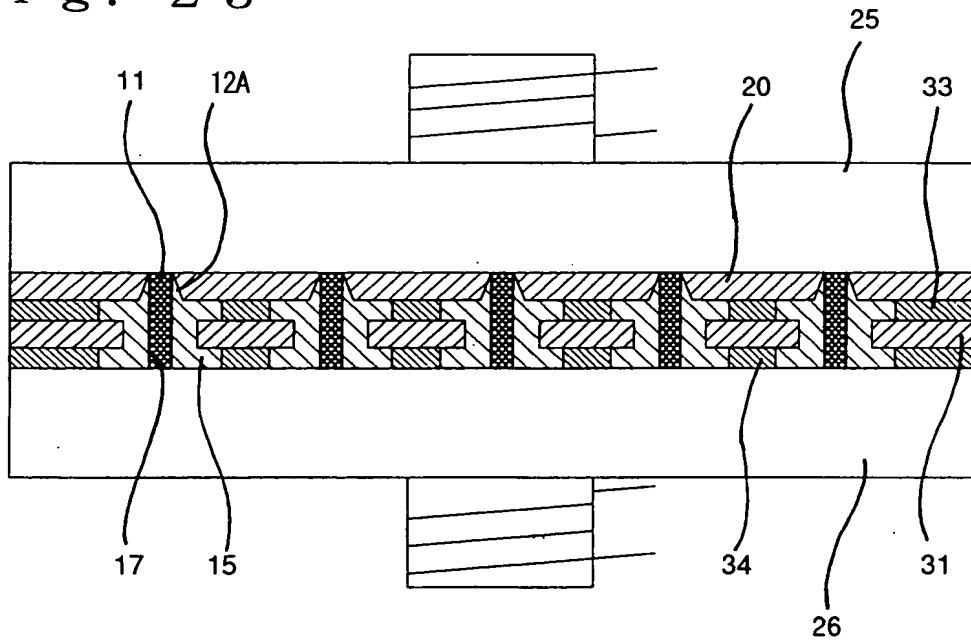
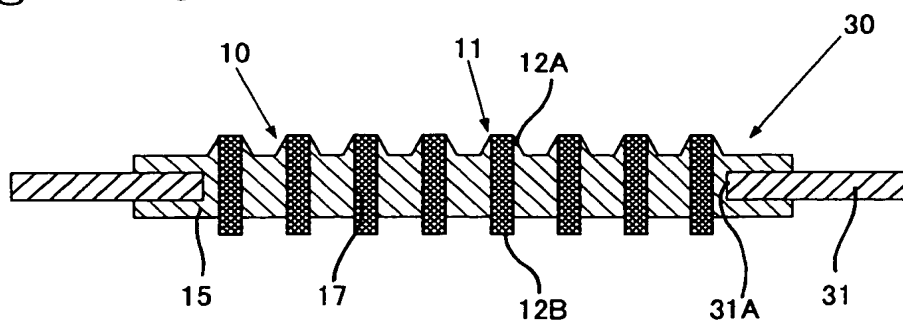


Fig. 25

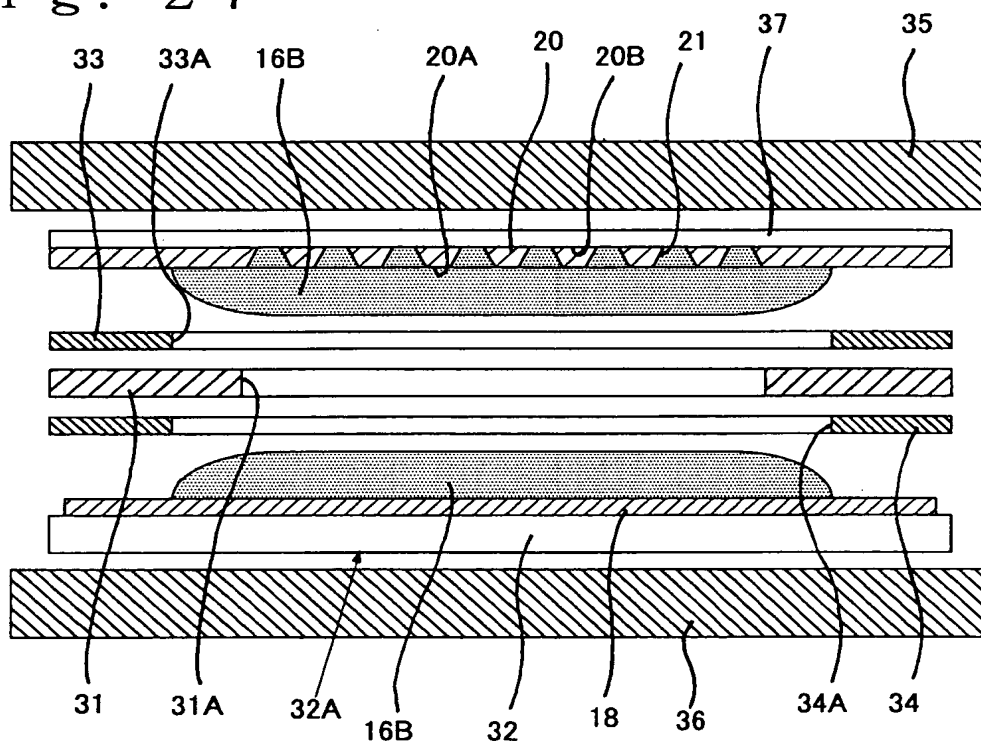




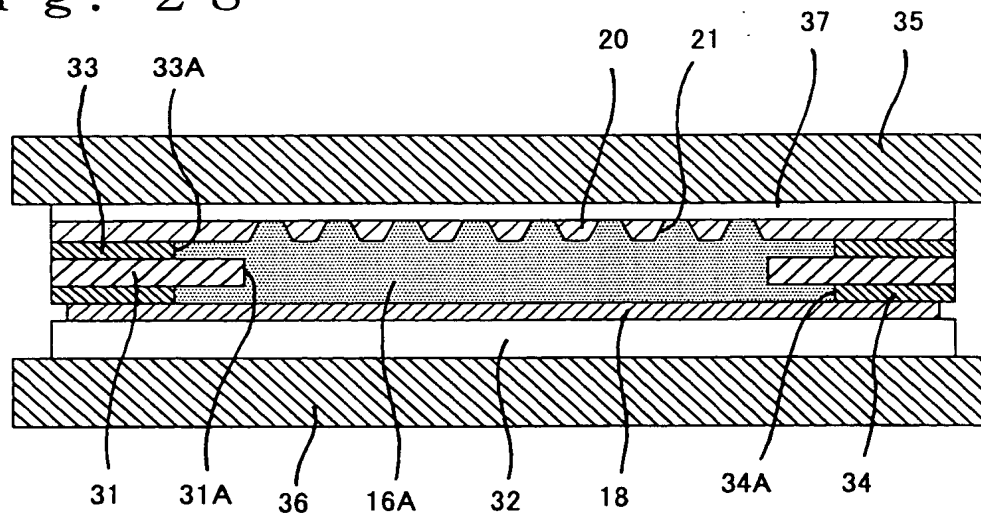
F i g . 2 6



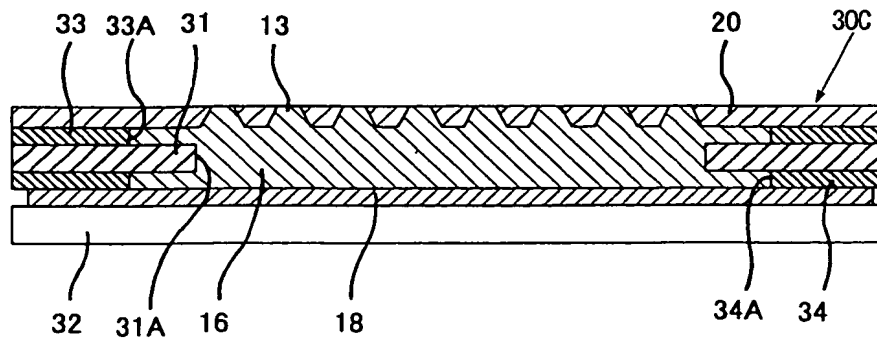
F i g . 2 7



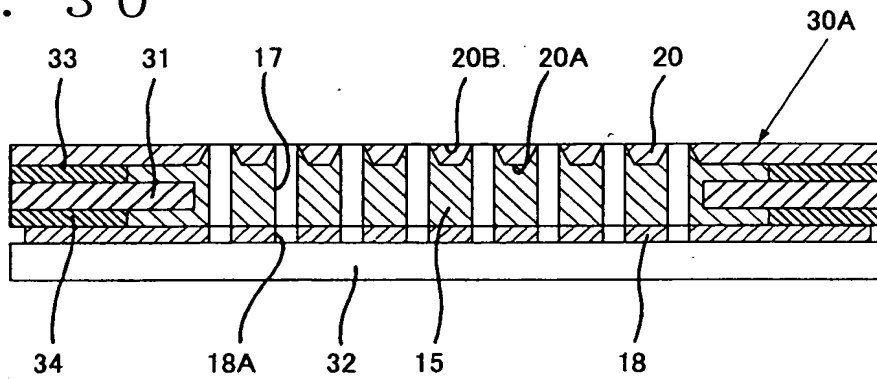
F i g . 2 8



F i g . 2 9



F i g . 3 0



F i g . 3 1

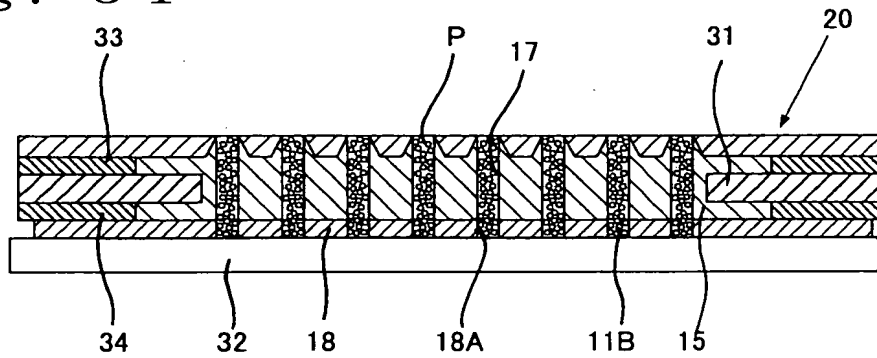


Fig. 32

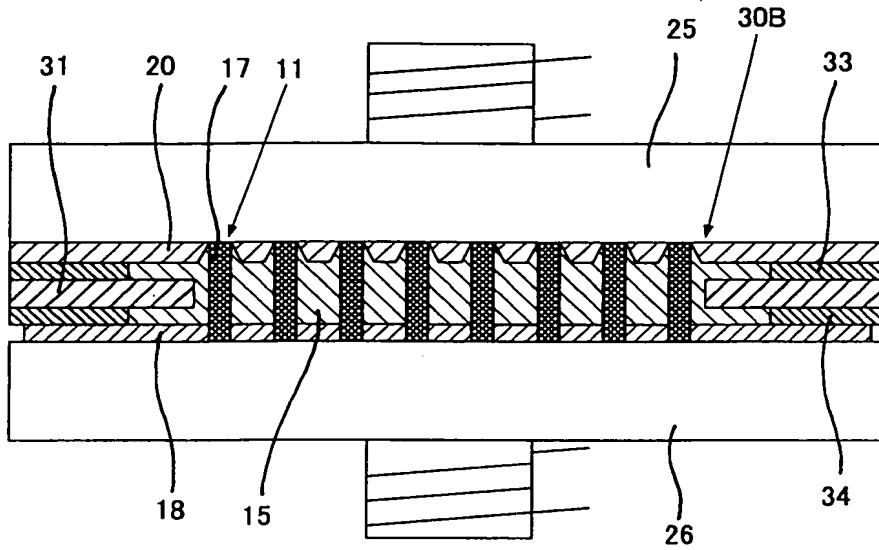


Fig. 33

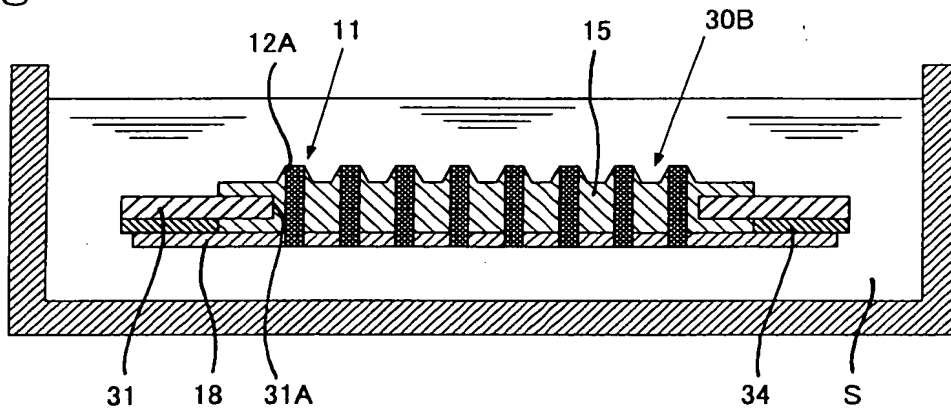
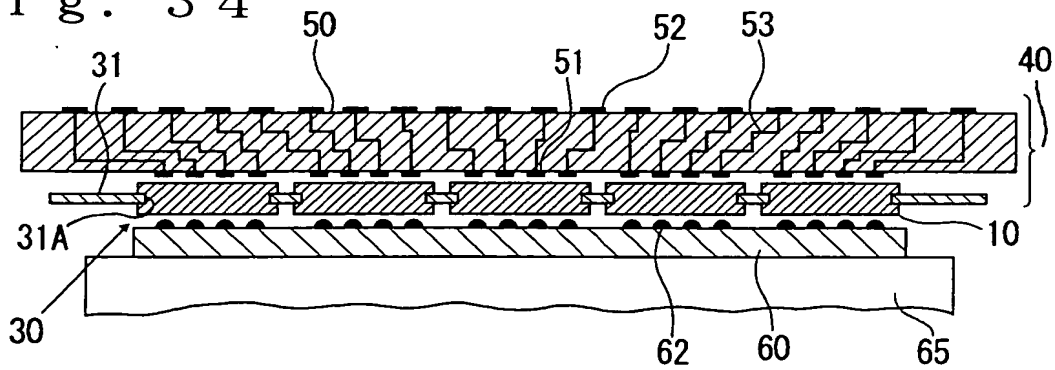
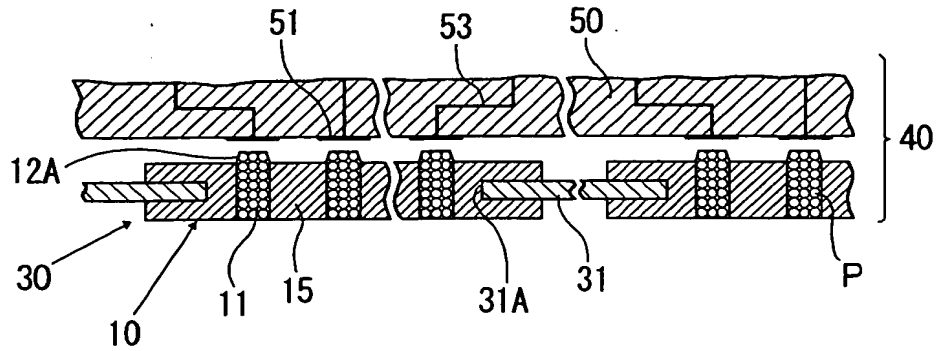


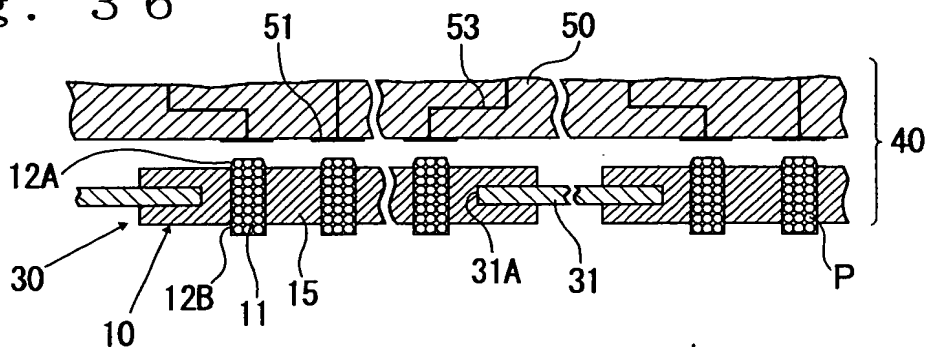
Fig. 34



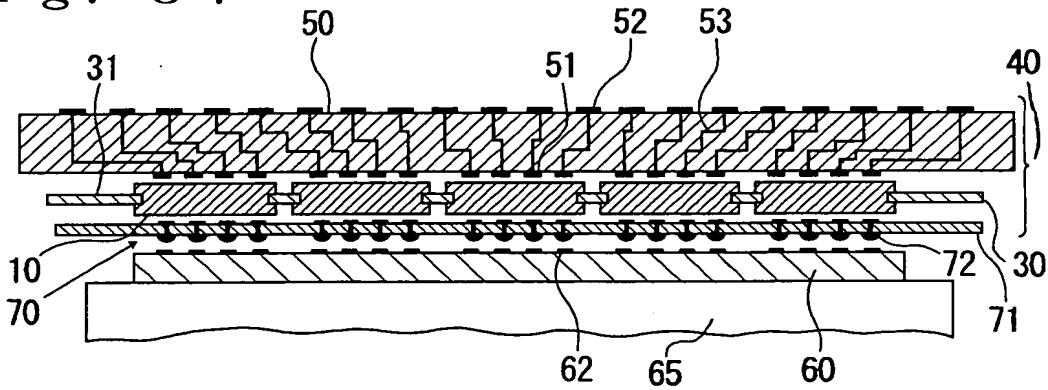
F i g . 3 5



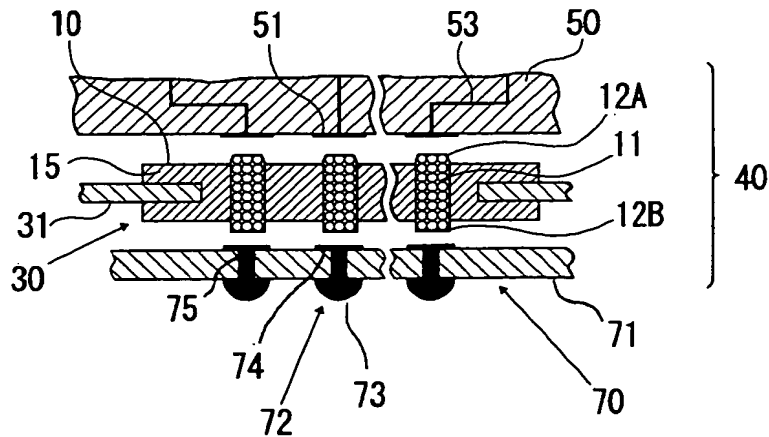
F i g . 3 6



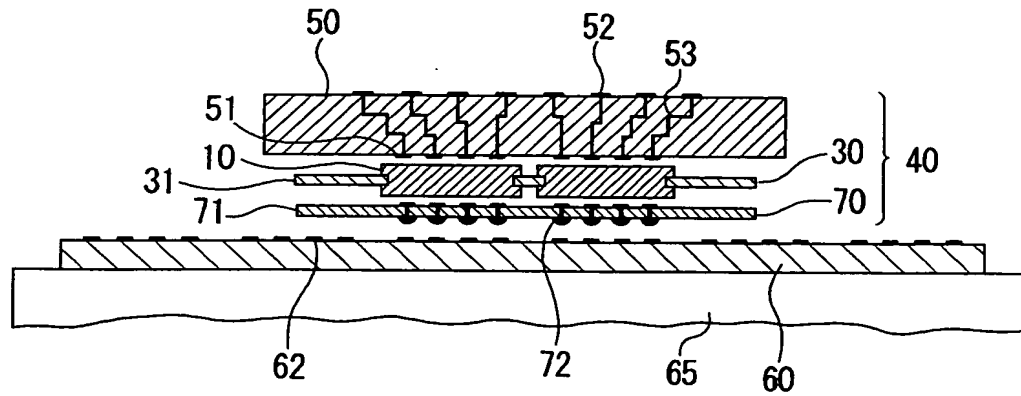
F i g . 3 7



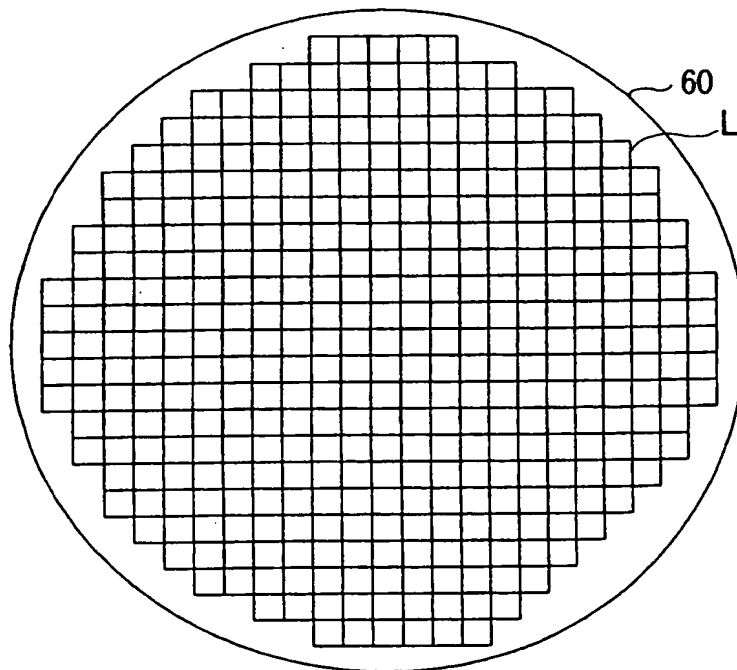
F i g . 3 8



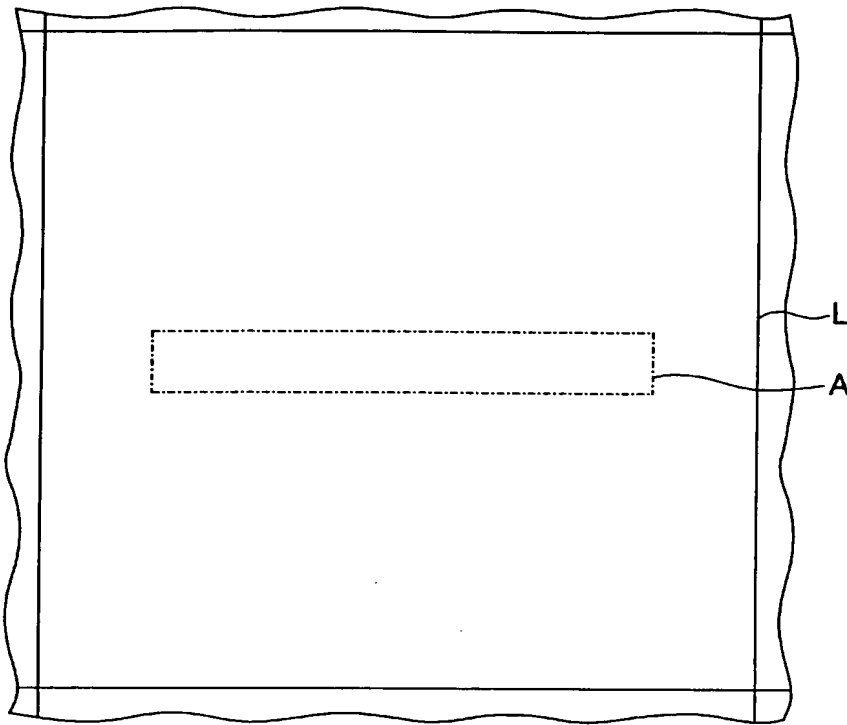
F i g . 3 9



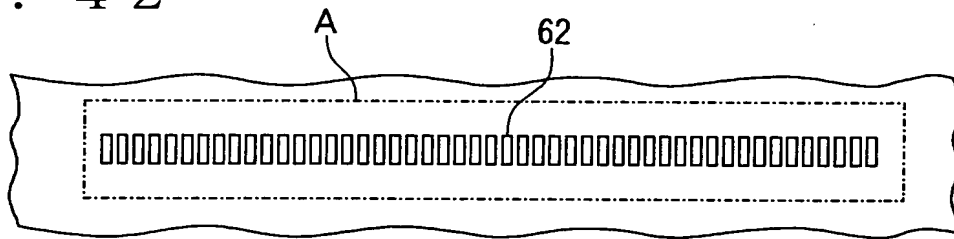
F i g . 4 0



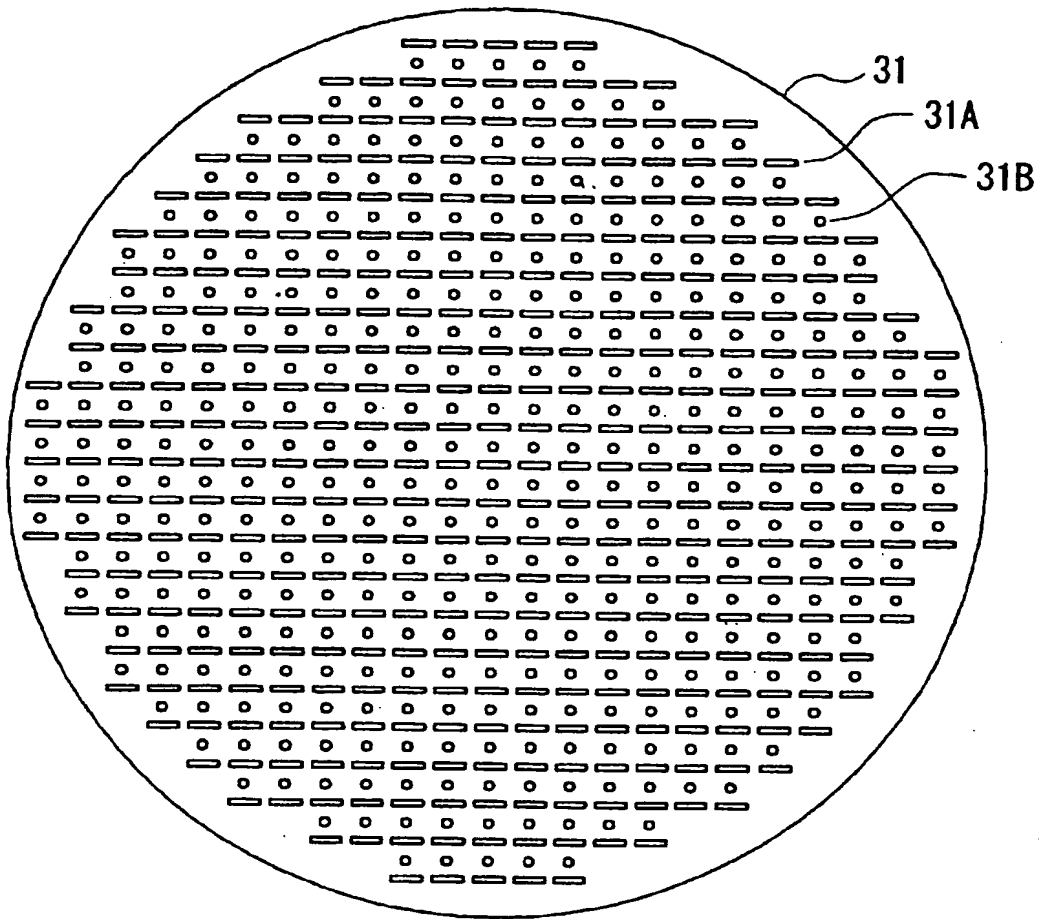
F i g . 4 1



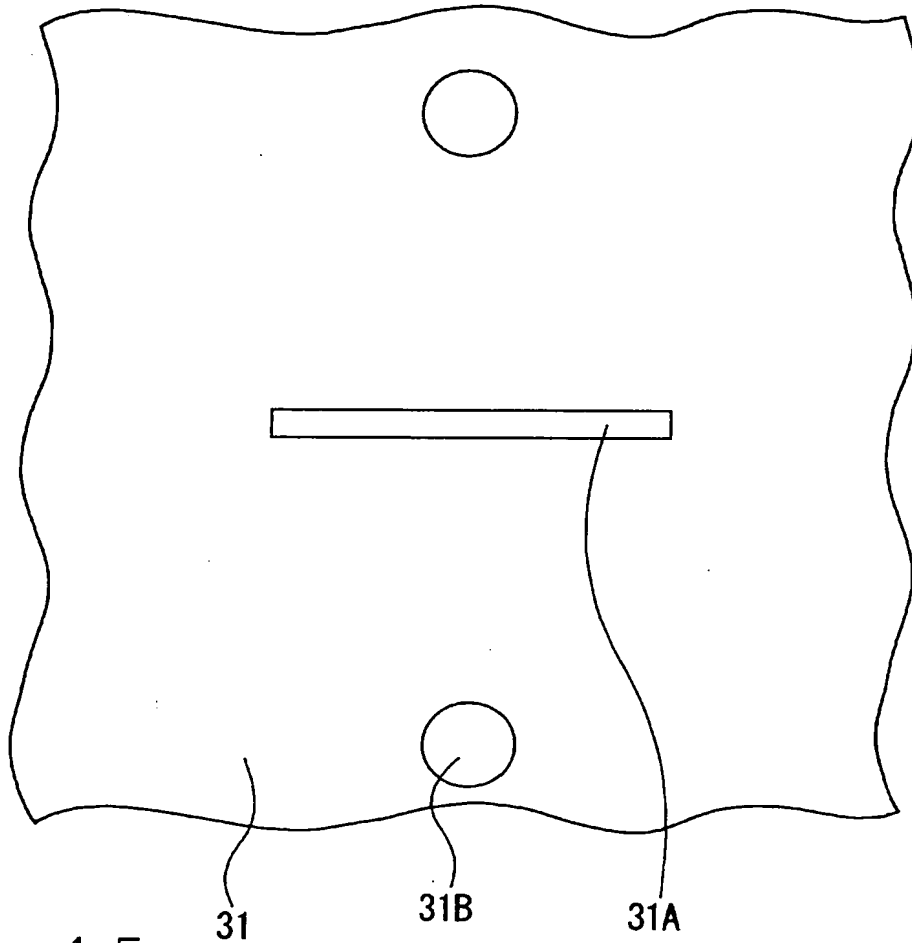
F i g . 4 2



F i g . 4 3



F i g . 4 4



F i g . 4 5

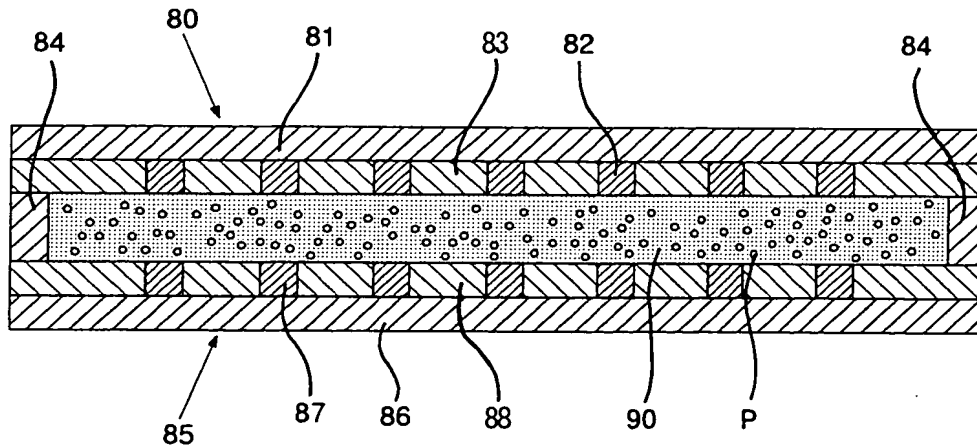




Fig. 46

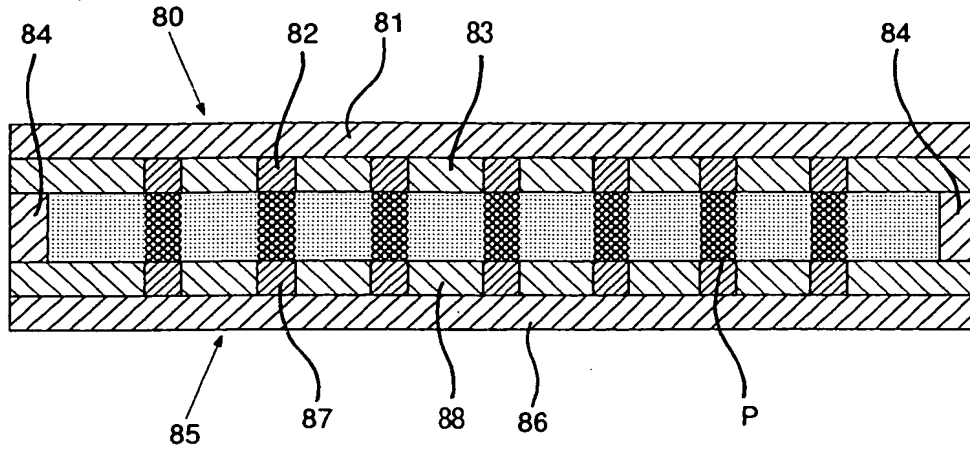


Fig. 47

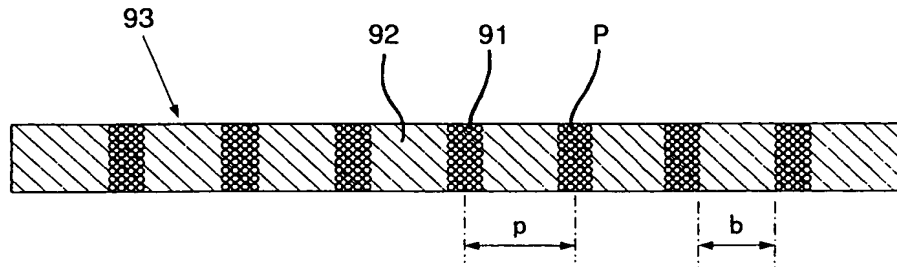


Fig. 48

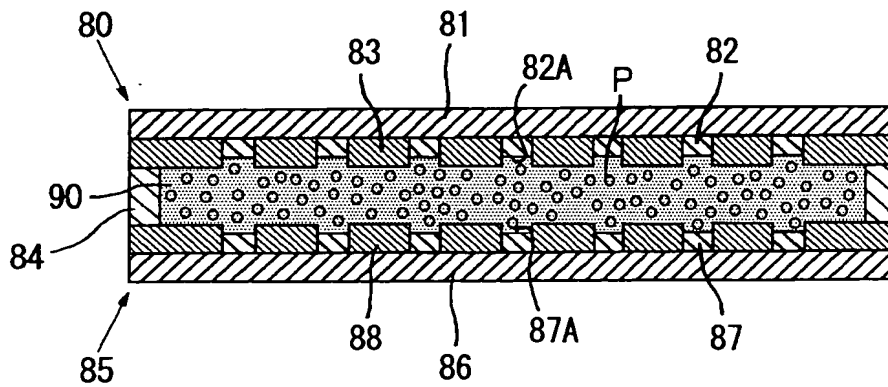
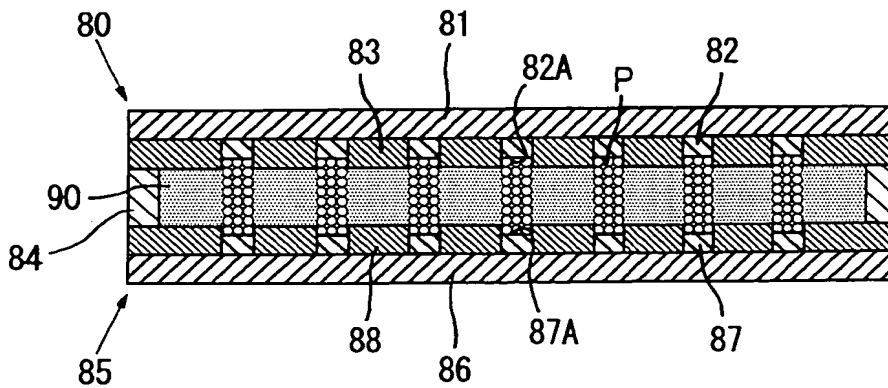
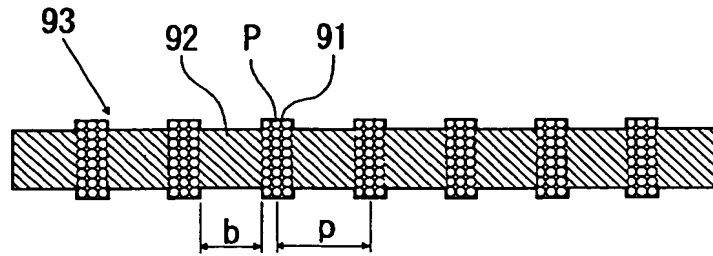


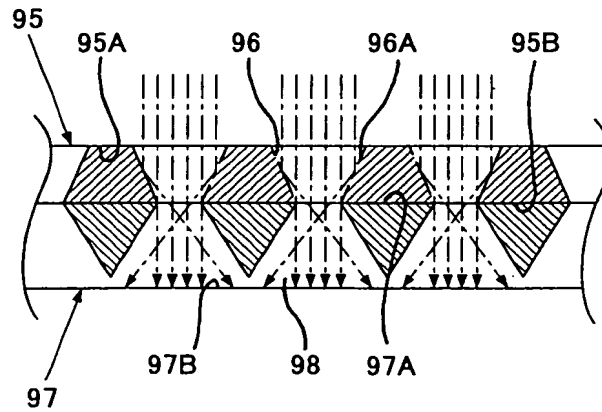
Fig. 49



F i g . 5 0



F i g . 5 1



F i g . 5 2

